



OFFICE OF THE REGISTRAR MANIPUR TECHNICAL UNIVERSITY, IMPHAL

(A University established under the Manipur Technical University Act, 2016)
Recognised by UGC under Section 2(f) and Section 22 of UGC Act, 1956
www.mtu.ac.in

REGULATIONS (COURSES AND SYLLABI FOR MASTER OF TECHNOLOGY PROGRAMS IN ELECTRONICS & COMMUNICATION ENGINEERING)

NOTIFICATION

Imphal, 7th September, 2026

AC-MTU-1/2/2026-MTU-MTU: It is notified to all that in exercise of the powers conferred by Section 45 of the Manipur Technical University Act, 2016, on recommendation of Board of Studies and as approved by the Academic Council of Manipur Technical University in its 9th meeting held on 30th May, 2026, hereby makes the following Regulations (Courses and Syllabi of Master of Technology program in Electronics & Communication Engineering), namely:-

1. Short title and commencement:

- (a) These Regulations may be called the Regulations (Courses and Syllabi for Master of Technology program in Electronics & Communication Engineering) 2026
- (b) They shall come into effect from the academic session 2026-27

2. Definitions:

- (1) In these Regulations, unless the context otherwise requires, -
 - (a) “Act” shall mean the Manipur Technical University Act, 2016
 - (b) “Board of Studies” means the board of studies of a Department
 - (c) “L”, “T”, “P”, “C”, shall mean respectively lecture hours per week, tutorial class hours per week, practical/ lab hours per week, credits per week.

(2) Words and expressions not defined in the Regulations but defined in the Statutes and Ordinances shall have the same meanings as assigned to them in the Statutes and Ordinances.

3. The Course Structure for the Master of Technology program in Electronics & Communication Engineering-

The Course Structure for the Master of Technology program in Electronics & Communication Engineering shall be as follows, with the detailed course for I semester, II semester, III semester and IV semester along with contents as given at Appendix.

ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT
MANIPUR TECHNICAL UNIVERSITY
[A University established under the Manipur Technical University Act, 2016]
Takyelpat, Imphal West, Manipur-795004
Website: www.mtu.ac.in

Curriculum and Syllabus
for
M. Tech.
In
“Microelectronics & VLSI Design”



MANIPUR TECHNICAL UNIVERSITY,
TAKYELPAT IMPHAL - 795004

Programme Learning Outcome (PLO)		
Sl. No.	Element of the Descriptor	Programme Learning Outcome
PLO1	Knowledge and understanding	Exhibit a coherent, foundational understanding of the field of Electronics and Communication Engineering, including its various learning areas, applications, and relationships with other disciplinary areas.
PLO2	Knowledge and understanding	Engage in hands-on laboratory work and practical activities that effectively prepare students for professional employment in Electronics and Communication Engineering, including roles in research and development, teaching, government or public service, and private or NGO sectors.
PLO3	Skills related to one's specialization	Effectively apply knowledge from core and related subfields of Electronics and Communication Engineering in multiple contexts, including preparation for advanced academic study in a chosen specialization.
PLO4	Application of knowledge and skills	Identify and apply suitable principles and methodologies to solve various types of Electronics and Communication Engineering problems that have well-defined solutions.
PLO5	Generic learning outcomes	Clearly and precisely report the results of experiments or investigations, and relate the conclusions or findings to the relevant theories and principles of Electronics and Communication Engineering, demonstrating a clear connection between practical outcomes and established theoretical frameworks in the field.
PLO6	Generic learning outcomes	Examine experimental results or findings and build logical arguments using appropriate technical language from Electronics and Communication Engineering. Clearly interpret the data, draw reasoned conclusions, and express them with the correct disciplinary terminology to demonstrate a strong command of the field's communication standards.

*** Rating Scale for CLO-PLO Mapping:**

3 – High Correlation,

2 – Moderate Correlation,

1 – Low Correlation

Course Structure for M.Tech. in Microelectronics and VLSI Design

Semester I							
S. No.	Category	Code	Course	L	T	P	Credits
1.	PCC	EC501	Research Methodology & Intellectual Property Rights	4	0	0	4
2.	PCC	EC502	Semiconductor Device & Modeling	3	0	0	3
3.	PCC	EC503	Digital VLSI Design	3	0	0	3
4.	PCC	EC504	Digital VLSI Design Lab	0	0	2	1
5.	PCC	EC505	Microelectronics Lab	0	0	2	1
6.	PEC	EC5xx	Elective I	3	0	0	3
7.	PEC	EC5xx	Elective II	3	0	0	3
8.	OEC	XXxxx	OEC I	2	0	0	2
Total contact hours/credits				18	0	4	20

Semester II							
S. No.	Category	Code	Course	L	T	P	Credits
1.	PCC	EC506	VLSI Technology	3	0	0	3
2.	PCC	EC507	Analog VLSI Design	3	0	0	3
3.	PCC	EC508	VLSI System Design and Verification	3	0	0	3
4.	PCC	EC509	Analog VLSI Design Lab	0	0	2	1
5.	PCC	EC510	VLSI System Design and Verification Lab	0	0	2	1
6.	PCC	EC511	Seminar	0	0	2	1
7.	PEC	EC5xx	Elective III	3	0	0	3
8.	PEC	EC5xx	Elective IV	3	0	0	3
9.	OEC	XXxxx	OEC II	2	0	0	2
Total contact hours/credits				17	0	6	20

Note:

- Exit option to qualify for a **PG Diploma in Microelectronics and VLSI Design**: Students opting for the exit option must complete a six- to eight-week industrial/academic training from a reputed industry.
- Continuation for **M. Tech. in Microelectronics and VLSI Design**: Students who continue in the program must also complete a four- to six-week industrial/academic training during the vacation.

Semester III							
S. No.	Category	Code	Course	L	T	P	Credits
1.	SI	EC601	Summer Internship Evaluation	-	-	-	2
2.	PRP	EC602	Project Phase I	0	0	36	18
Total contact hours/credits				0	0	36	20

Semester IV							
S. No.	Category	Code	Course	L	T	P	Credits
1.	PRP	EC603	Project Phase II	0	0	40	20
Total contact hours/credits				0	0	40	20

List of Electives		
Elective I		
S. No.	Code	Course
1.	EC520	Memory Technologies
2.	EC521	Nanoelectronics
3.	EC522	DSP Architectures and Embedded Systems
4.	EC523	MEMS Analysis
5.	EC524	MIC & MMIC
Elective II		
S. No.	Code	Course
1.	EC530	CAD for VLSI Design
2.	EC531	Optoelectronic Devices
3.	EC532	Low Power VLSI Design
4.	EC533	RF Design
5.	EC534	RF Solid State Device
OEC I		
1.	EC540	English for Technical Writing
2.	EC541	Fundamentals of IoT
Elective III		
S. No.	Code	Course
1.	EC550	AC Analysis of MOS
2.	EC551	Mixed Signal VLSI Design
3.	EC552	Advanced Computer Architecture and Processor Design
4.	EC553	Solar Photovoltaics and Thin Film Technology
5.	EC554	5G Communication Technology
Elective IV		
S. No.	Code	Course
1.	EC560	System on Chip Design
2.	EC561	Reconfigurable Hardware Design
3.	EC562	Advanced CMOS Devices and Technology
4.	EC563	Flexible Electronics
OEC II		
S. No.	Code	Course
1.	EC571	IKS in Electronics Engineering
2.	EC572	Introduction to Drone Technology

Notes:

1. Any course of 8/12 weeks offered by Swayam - NPTEL can be opted during the respective semester as electives with the prior approval from the Program Coordinator.
2. A list of electives offered in each semester will be announced by the Departments based on the requirements and availability of faculty.
3. The evaluation (Online elective courses) will be based on assignments and internal assessments conducted by the concerned course instructor and examinations as per the MTU Ordinance of Postgraduate Programmes leading to the Degrees of Master of Technology.
4. Internship Evaluation will be performed based on presentation within 1st month of 3rd semester.
5. Project Phase II is the continuation of Project Phase I.

**SEMESTER I
M.TECH.
IN
MICROELECTRONICS AND VLSI DESIGN**

Code	Course	L	T	P	C
EC501	Research Methodology & Intellectual Property Rights	4	0	0	4

Course Outcomes:

At the end of this course, students will be able to

CLO1. Understand research problem formulation.

CLO2. Analyze research related information

CLO3. Follow research ethics

CLO4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.

CLO5. Understanding that when IPR would take such important place in growth of individuals & Nation, it is needless to emphasis the need of information about Intellectual Property

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	2	2	1	2
CLO2	3	2	3	2	2	3
CLO3	2	2	1	-	2	2
CLO4	2	1	3	2	1	2
CLO5	2	1	2	1	1	1

Syllabus Contents:

Module 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

Module 2: Effective literature studies approaches, analysis Plagiarism, Research ethics.

Module 3: Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

Module 4: Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Module 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Module 6: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & Engineering students".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction".
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step-by-Step Guide for beginners".
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.
5. Mayall, "Industrial Design", McGraw Hill, 1992.
6. Niebel, "Product Design", McGraw Hill, 1974.
7. Asimov, "Introduction to Design", Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
9. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Code	Course	L	T	P	C
EC502	Semiconductor Device & Modeling	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

- CLO1. Apply the fundamental principles of semiconductor physics to design modern electronic devices and their applications
- CLO2. Analyze the basic semiconductor device physics
- CLO3. Demonstrate quantum mechanics and its applications in semiconductor devices.
- CLO4. Illustrate band engineering of devices
- CLO5. Demonstrate modeling and simulation of semiconductor devices

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	3	3	1	2
CLO2	3	2	3	3	2	3
CLO3	3	1	3	2	-	2
CLO4	3	2	3	2	1	2
CLO5	3	3	3	3	2	3

Syllabus Contents:

Module 1: Semiconductor Electronics: Semiconductor Materials, Band Model of Solids Thermal-Equilibrium Statistics, Carriers in Semiconductors, Drift Velocity, Mobility and Scattering, Drift & Diffusion Current, Device: Hall-Effect.

Module 2: Metal-Semiconductor Contacts And P-N Junctions: Metal-Semiconductor junctions, Current-Voltage Characteristics, Surface Effects. The p-n junction, Step Junction, Linearly Graded Junction, Heterojunctions, Reverse-Biased p-n junctions and break down mechanism. Generation and Recombination.

Module 3: Field-Effect Transistors (MOSFETs): MOS Capacitor, Flat Band Voltage, Oxide and Interface Charge, High and Low Frequency C-V Characteristics, Basic MOSFET behavior, Threshold Voltage Model, 1st Order I-V Model.

Module 4: Short Channel Effects: Moore's law, Technology nodes and ITRS, Physical & Technological Challenges to scaling short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, subthreshold current, hot carrier effects, velocity overshoot, high field effects in scaled MOSFETs, substrate current and effects in scaled MOSFETs.

Module 5: Nonconventional MOSFETs: High-k/metal gate, high mobility MOSFETs, SOI, Multi-gate MOSFETs, FinFET, GAA MOSFETs. Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations.

Textbook(s):

1. D. A. Neamen, Semiconductor Physics and Devices, McGraw Hill Education, 4th Edition, 2021

2. D. J. Griffiths, Introduction to Quantum Mechanics, Cambridge University Press, Third Edition, 2018

Reference Books:

1. R. L. Liboff, Introductory Quantum Mechanics, Pearson, 4th Edition, 2003
2. N. W. Ashcroft and N. D. Mermin, Solid State Physics, Brooks, 2021
3. J. P. Mckelvey, Solid State and Semiconductor Physics, Harper and Row, 1966.
4. D.K. Schroder, Semiconductor Material and Device Characterization, John Wiley, 1990.
- C.T.Sah, Fundamentals of Solid-State Electronic Devices, Allied Pub. & World Scientific, 1991.

Code	Course	L	T	P	C
EC503	Digital VLSI Design	3	0	0	3

Course Learning Outcomes:

At the end of this course, students will be able to

- CLO1. Design a CMOS inverter meeting the static and dynamic performance characteristics.
- CLO2. Design combinational logic circuits (both static and dynamic) in CMOS.
- CLO3. Design sequential logic circuits in CMOS.
- CLO4. Design various Arithmetic Building Blocks.
- CLO5. Carryout the layout design using CAD tools.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	3	3	3	1	2
CLO2	3	3	3	3	-	2
CLO3	3	3	3	3	-	2
CLO4	3	3	3	3	1	2
CLO5	3	3	3	3	2	3

Syllabus Contents:

Module 1: Review of MOSFET operation and CMOS process flow: MOS Threshold voltage, MOSFET I-V characteristics: long and short channel, MOSFET capacitances, lumped and distributed RC model for interconnects, transmission lines, CMOS process flow, Layout and design rules.

Module 2: CMOS inverter: Static characteristics, power consumption, dynamic behaviour, buffer design using the method of logical effort.

Module 3: Combinational logic: Transistor sizing in static CMOS logic gates, static CMOS logic gate sizing considering method of logical effort, dynamic logic, pass-transistor logic, common mode and other cross- coupled logic families.

Module 4: Sequential logic: Static latches and flip-flops (FFs), dynamic latches and FFs, sense-amplifier based FFs, NORA-CMOS, Schmitt trigger, monostable and astable circuits.

Module 5: Memories and array structures: MOS-ROM, SRAM cell, memory peripheral circuits

Text Book:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentice Hall, 2003.
2. Sung-Mo Kang, Yusuf Liblebici, "CMOS Digital Integrated Circuits," Tata Mc Graw

Hill, 2003.

Reference Books:

1. R. Jacob Baker, “CMOS Mixed-Signal Circuit Design,” Wiley India Pvt. Ltd, 2009
Ivan Sutherland, R. Sproull and D. Harris, “Logical Effort: Designing Fast CMOS Circuits”,
Morgan Kaufmann, 1999.

Code	Course	L	T	P	C
EC504	Digital VLSI Design Lab	0	0	2	1

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Learn the fundamental principles of VLSI circuit design in digital domain.

CLO2. Use industry standard EDA tools to design digital VLSI circuits.

CLO3. Design and simulate basic CMOS logic circuits using VLSI design tools.

CLO4. Implement combinational and sequential circuits using hardware description languages (HDL) and CAD tools.

CLO5. Perform layout design, verification, and testing of digital integrated circuits.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	2	-	-
CLO2	2	3	3	2	1	1
CLO3	2	3	3	3	1	2
CLO4	2	3	3	3	2	2
CLO5	2	3	3	3	2	3

Syllabus Contents:

List of Experiments:

1. Study and analysis of the CMOS Inverter circuits.
2. Study and analysis of Static CMOS logic gates.
3. Study and analysis of Dynamic CMOS logic gates.
4. Implementation of given Boolean expression in various logics and its analysis.
5. Combinational logic circuits design implementation.
6. Sequential logic circuits design implementation.

Code	Course	L	T	P	C
EC505	Microelectronics Lab	0	0	2	1

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Understand the mathematical model of junction and devices.

CLO2. Design photo-detector and solar cell devices.

CLO3. Measure and analyze the device performance

CLO4. Design innovative microelectronic device.

CLO5. Develop practical skills in fabrication, analysis, and performance evaluation of microelectronic circuits.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	-	2	2	-	1
CLO2	2	2	3	3	-	1
CLO3	2	3	2	3	2	3
CLO4	2	2	3	3	1	2
CLO5	2	3	3	2	3	3

Syllabus Contents:

The laboratory course consists of the following experiments:

1. Electrical characterization of fabricated P-N Junction Diodes: I-V measurement and extraction of parameter like V_{bi} , leakage current etc.
2. Fabrication of Metal-Oxide thin film and Metallization on Si wafer to form MOS capacitor
3. Electrical characterization of MOS capacitor: I-V and extraction of parameter like gate leakage current,
4. C-V measurement of MOS capacitor (at high frequency and low frequency) and extraction of parameter like gate leakage current, flat band voltage etc.
5. Solar cell characterization i.e. J-V (light/dark), efficiency calculation.
6. Characterization of Photodetector and calculation of parameters like responsivity, detectivity etc.
7. Characterization and analysis of Sensor devices
8. Modeling and simulation of semiconductor device using MATLAB.

Code	Course	L	T	P	C
EC520	Memory Technologies	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1 Select architecture and design semiconductor memory circuits and subsystems.

CLO2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.

CLO3. Knowhow of the state-of-the-art memory chip design.

CLO4. Analyze the architecture, operation, and performance characteristics of volatile memories such as SRAM and DRAM.

CLO5. Describe the working principles, fabrication aspects, and applications of non-volatile memories including ROM, PROM, EEPROM, and Flash memory.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	3	3	-	2
CLO2	3	2	2	3	2	3
CLO3	3	1	2	2	1	2
CLO4	3	2	3	3	2	3
CLO5	3	1	2	2	1	2

Syllabus Contents:

Module 1: Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Module 2: DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

Module 3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Module 4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Module 5: Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs)

FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Module 6: Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

References:

- Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience.
- Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition.
- Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI.

Code	Course	L	T	P	C
EC521	Nanoelectronics	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Apply the concept of non-classical MOS transistor to solve the issues associated with scaling.

CLO2. Realize advanced FET devices.

CLO3. Design of emerging device like FinFET, Trigate FET, etc.

CLO4. Determine suitable fabrication process to grow thin film and nanomaterial devices.

CLO5. Understand tools to characterize nano-materials and thin film devices.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	2	2	2	3	1	2
CLO2	3	3	3	2	1	1
CLO3	2	3	2	3	1	2
CLO4	2	2	2	1	2	2
CLO5	3	2	-	-	1	1

Syllabus Contents:

Module 1: Review of the fundamentals of Quantum Mechanics – From classical electronics to nanoelectronics; Electronic properties of low dimensional structures – quantum wells, quantum wires, quantum dots, Plasmonic effect of nanoparticle.

Module 2: Fundamental of MOSFET Structure: Fundamentals of Silicon MOSFET Devices, scaling rules, Gate oxide tunneling and hot electron effects in nano MOSFET,

Module 3: Emerging Device: Advanced MOSFETS- Trigate FETs, FinFETs-CMOS, Nanowire FET, CNT and Graphene Transistors. Coulomb blockage, single electron transfer devices (SETs), Tunnel FET, Quantum dot array, Quantum computer.

Module 4: Synthesis of Nanomaterials: Nanomaterials: Nanowires, Nanotubes, nanorods, nanoparticle and other nano structures, CVD- MOCVD and Plasma CVD, Nucleation and Growth, ALD, Epitaxy, MBE. Compound semiconductor hetero-structure growth. Optical-reflectance and ellipsometry

Module 5: Characterizations of Nanomaterials: Characterization techniques for nanomaterials: FTIR, XRD, AFM, SEM, TEM, EDAX etc.

Textbooks:

1. Mark Lundstrom and Jing Guo: Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005
2. Karl Goser: Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005

3. S. K. Ghandhi, VLSI fabrication principles,” 2nd Edition, Wiley-India,

Reference Books:

1. Fundamentals of Modern VLSI Devices, Y. Taur and T. Ning, Cambridge University Press, Third Edition. 2022
2. Silicon VLSI Technology, Plummer, Deal, Griffin, Pearson Education India, First Edition, 2009
3. Encyclopedia of Materials Characterization, Edited by: Brundle, C. Richard; Evans, Charles A. Jr.; Wilson, Shaun; Elsevier, First Edition 1992.

4.

Code	Course	L	T	P	C
EC522	DSP Architectures and Embedded Systems	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Recollect digital transform techniques.

CLO2. Differentiate between the architectural features of General-purpose processors and DSP processors.

CLO3. Design, implement, analyze and compare digital filters for processing of discrete time signals.

CLO4. Comprehend the architectures of TMS320C64XX devices and acquire knowledge about various addressing modes of DSP TMS320C64XX.

CLO5. Apply multirate signal processing techniques and DSP processor architectures for efficient implementation of real-time signal processing applications.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	2	1	2
CLO2	3	1	2	2	1	2
CLO3	3	3	3	3	2	3
CLO4	3	2	3	2	-	2
CLO5	3	3	3	3	2	3

Syllabus Contents:

Module 1: Orthogonal Transforms: Discrete Fourier Transform, Properties of DFT, Computation of DFT, FFT Decimation in time, Decimation in frequency; Linear convolution using DFT, Discrete Cosine Transform and Haar Transform.

Module 2: Digital Filter Structures: Basic FIR/IIR filter structures, FIR/IIR Cascaded lattice structures, Parallel realization of IIR transfer functions, Computational complexity of filter structures; Adaptive Filter Algorithms - LMS and RLS, Introduction to Kalman Filtering.

Module 3: Multi-Rate Signal Processing: Basic structures for sampling rate conversion, Decimators and Interpolators; Multistage design of interpolators and decimators; Polyphase decomposition and FIR structures; Different interpolation algorithms-Lagrange interpolation, Spline interpolation; Applications in sub-band coding.

Module 4: Digital Signal Processors Introduction: Computational characteristics of DSP algorithms and applications; Techniques for enhancing computational throughput: Harvard architecture, parallelism, pipelining, dedicated multiplier, split ALU and barrel shifter.

Module 5: TMS320C64XX Architecture: CPU data paths and control, general purpose register files, register file cross paths, memory load and store paths, data address paths, parallel operations and resource constraints.

Textbooks:

1. R. Chassaing and D. Reay, Digital signal processing and applications with TMS320C6713 and TMS320C6416, Wiley, 2008.
2. S. K. Mitra, Digital Signal Processing: A Computer Based Approach, 3rd Edition, TMH, 2008.
3. J. G. Proakis and D. G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Pearson Prentice Hall, 2007.

Code	Course	L	T	P	C
EC523	MEMS Analysis	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

- CLO1. Understand the fundamentals, fabrication process and applications of MEMS.
- CLO2. Understand the basic principles of MEMS sensors and actuators (mechanical, electrical, piezo resistive, piezoelectric, thermal, microfluidic).
- CLO3. Understand the application of beam mechanics and material properties for the design of various sensors and actuators.
- CLO4. Gain the idea of base of various MEMS sensors and actuators.
- CLO5. Implement various applications of MEMS in Biomedical field and healthcare domain and also investigate CMOS-MEMS integration in VLSI domain.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	1	2	1	1
CLO2	3	2	2	2	-	1
CLO3	2	2	3	3	2	2
CLO4	2	2	3	3	2	3
CLO5	2	3	3	3	2	2

Syllabus Contents:

Module 1: Introduction: What is MEMS? Unique Characteristics of MEMS and Typical Application Areas of MEMS.

Module 2: IC fabrication vs. MEMS Fabrication: Deposition, lithography, oxidation, etching, Plasma etching, Sputtering, RIE, 1, 2 and 3 mask level processes, wet etching (anisotropic and isotropic), crystal directions in Si, Bulk micro-machining, Surface micro-machining, wafer bonding, Electroplating, Molding, etc.

Module 3: Introduction to Beam Mechanics: Relationship between tensile stress and strain, mechanical properties of silicon and thin films, Flexural beam bending analysis under single loading condition, types of beam, deflection of beam, longitudinal strain under pure bending spring constant, torsional deflection, intrinsic stress, resonance and quality factor.

Module 4: Sensing and Actuation: Electrostatic sensing and actuation, parallel plate capacitor, Application, inertial, pressure and tactile sensor parallel plate actuator, comb drive. Thermal sensing and Actuators, thermal sensors, Actuators – Applications, Inertial, Flow and Infrared sensors. Piezoresistive sensors, piezoresistive sensor material, stress in

flexural cantilever and membrane Application, Inertial, pressure, flow and tactile sensor. Piezoelectric sensing and actuation, piezoelectric material properties, quartz, PZT, PVDF–ZnO Application, Inertial, Acoustic, tactile, flow, surface elastic waves. Magnetic actuation, Micro magnetic actuation principle, deposition of magnetic materials, Design and fabrication of magnetic coil.

Module 5: Electrothermal MEMS: Flow Sensors, Gas Detectors, Uncooled Infrared Sensors, Bimorph Actuators, Bent-Beam Actuators.

Module 6: RF MEMS: Switches, active and passive components, static and dynamic modeling. CMOS-MEMS Integration: Overview, different techniques, packaging and integration.

Module 7: Overview of BioMEMS, Microfluidics: Biosensor and BioMEMS, Microfluidics, Digital Microfluidics, Ink jet printer.

Textbooks:

1. Chang Liu, Foundations of MEMS, Pearson Education Asia, 2012.
2. S. D. Senturia, Microsystem Design, Springer, India, 2006.

Code	Course	L	T	P	C
EC524	MIC & MMIC	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Understand the concept of hybrid and monolithic MIC technology.

CLO2. Understand the characterisation and design of microstrip integrated circuits.

CLO3. Understand the concept of coupled microstrip and directional couplers.

CLO4. Able to analyse and design MIC using lumped elements- high power and low power circuits.

CLO5. Study about microstrip circulator, isolators and phase shifters.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	1	-	-
CLO2	3	2	3	3	1	2
CLO3	2	2	3	3	2	3
CLO4	2	3	3	3	2	2
CLO5	2	1	2	2	1	2

Syllabus Contents:

Module 1: MIC Technology – Thick film and Thin film technology, Hybrid MIC's, Monolithic MIC technology.

Module 2: Analysis of stripline and microstripline, Method of conformal Transformation, characteristic parameters of strip, Microstrip lines, Microstrip Circuit Design, Impedance transformers, Filters, Lumped constant Microstrip circuits.

Module 3: Coupled Microstrips and Directional couplers, Even and odd mode analysis, Theory of coupled microstrip, Directional couplers, Calculations for a coupled pair of Microstrips, Branch line couplers. Lumped Elements for MIC's Design and fabrication of lumped elements, circuits using lumped elements.

Module 4: Nonreciprocal components for MIC's Microstrip on Ferrimagnetic substrates, Microstrip circulators. Isolators and phase shifters, Design of microstrip circuits – high power and low power circuits.

Textbooks:

1. Microwave Devices & Circuits, By S Y Liao, Pearson.
2. Microwave Integrated circuits, By Gupta KC and Amarjit Singh - Wiley Eastern.
3. Stripline-like Transmission Lines for Microwave Integrated Circuits, By Bharathi, Bhat, and S.K. Koul, New Age International.

Code	Course	L	T	P	C
EC530	CAD for VLSI Design	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

- CLO1. Get the concept of total VLSI design style, starting from basic one-time programmable logic to Application Specific Integrated Circuit.
- CLO2. Exposed to know and explore different Algorithmic Approaches to solve complex problem related to High Level Synthesis of circuit behaviour to get efficient Register Transfer level realization using Computer Aided Software/Tools.
- CLO3. Know how efficiently delay of a big digital circuit will be estimated using logical effort and what will be the optimum stages to get the least delay.
- CLO4. Know the importance of Computer Aided (CAD) Automation for solving VLSI physical design problems and they will be able to develop their own CAD algorithms to solve physical design and Synthesis problems.
- CLO5. Understand the importance of VLSI circuit testing and different approaches of VLSI testing.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	2	1	1
CLO2	2	2	3	3	1	2
CLO3	2	1	2	3	2	3
CLO4	2	3	3	3	1	2
CLO5	2	2	2	2	2	3

Syllabus Contents:

Unit 1: Different types of VLSI design styles: Full custom, standard cell based, gate array based, programmable logic, field programmable gate arrays etc. VLSI Design flow. High level design (scheduling, allocation and binding), CAD tools for VLSI design.

Unit 2: Logical effort, path effort, logical effort calculation for different gates and circuits, logical effort to estimate minimum path delay, Logical effort of optimum transistor sizing.

Unit 3: VLSI Design automation-partitioning (problem formulation, cost function, different partitioning approach, Kernighan-Lin, Fiduccia-Mattheyses and simulated annealing heuristic for partition), Floor planning (problem definition, cost function, modeling floor planning problem, approach to solve floor planning), Placement (problem definition, cost function, approach to solve floor planning), Global routing, Detailed Routing-Maze routing, Channel routing.

Unit 4: Combinational & sequential logic simulation, logic synthesis, verification, high level Synthesis. synthesis issues and algorithms.

Unit 5: Importance of VLSI testing, Fault modeling, Design for testability, Fault simulation, Test generation.

References:

1. S. Ramachandran, "Digital VLSI systems design", Springer, 2007.
2. R.H. Katz, "Contemporary logic design", Addison-Wesley Pub. Co., 1993.
3. M.J.S. Smith, "Application-specific integrated circuits", Addison-Wesley Pub. Co., 1997.
4. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing", Kluwer Academic Publishers, 2000.
5. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems Testing and Testable Design", Wiley-IEEE Press, 1993.
6. High-Level Synthesis: from Algorithm to Digital Circuit, P. Coussy and A. Morawiec, Springer, 2008.
7. Sutherland, B. Sproull and D. Harris, Logical Effort: Designing Fast CMOS Circuits, Elsevier
8. M. Sarrafzadeh and C.K. Wong, "An introduction to physical design", McGraw Hill, 1996.
9. N.A. Sherwani, "Algorithms for VLSI physical design automation", Kluwer Academic Publishers, 1999.
10. S.M. Sait and H. Youssef, "VLSI physical design automation: theory and practice", World Scientific Pub. Co., 1999.

Code	Course	L	T	P	C
EC531	Optoelectronic Devices	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to

- CLO1. Explain key concepts in quantum and statistical mechanics relevant to physical, electrical and optoelectronic properties of materials
- CLO2. Analyze optoelectronic devices
- CLO3. Design photonic integrated circuits that emit, modulate, switch, and detect photons.
- CLO4. Describe fundamental and applied aspects of optoelectronic device physics and its applications.
- CLO5. Design an efficient solar cell based on given specifications

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	2	1	1
CLO2	2	3	3	3	2	2
CLO3	3	2	3	2	-	1
CLO4	3	2	1	1	-	-
CLO5	2	3	2	3	1	2

Syllabus Contents:

Module 1: Quantum Mechanics: Crystal structures, Particle in a box, Bandgap.

Module 2: Electronic structure of semiconductor heterostructures: Density-of-states: 3D, 2D, 1D, Effective mass, Heavy doping effect, Optical process in semiconductors.

Module 3: Heterojunction band alignment and quantum wells: Theory of band alignment, Drift-diffusion, Transport properties, Heterojunction diode current. Propagation of light.

Module 4: Semiconductor lasers and Photodetectors: Quantum well lasers, Vertical cavity surface emitting lasers, Quantum efficiency; gain and bandwidth; Integrated laser-modulator; multi-section phase; gain; Distributed Bragg reflector devices.

Module 5: Solar cells: Carrier recombination and lifetime, Carrier transport under illumination, Heterojunction III-V single and multijunction cells, Design of a multijunction solar cell.

Textbooks:

1. Pallab Bhattacharya “Semiconductor optoelectronic devices” Prentice Hall of India, Second Edition, 2002.
2. Jasprit Singh “Electronic & Optoelectronic properties of Semiconductor” Cambridge University Press, Second Edition, 2016

Reference Books:

1. J Wilson and J. F. B. Hawkers, “Optoelectronics - An introduction” Prentice Hall of India, Third edition 2017.

2. Jia-Ming Liu, Photonic Devices, Cambridge University Press, New York, First Edition 2005
3. Shun Lien Chuang; Physics of Photonic Devices, John Wiley & Sons, Second Edition, 2009
4. Nelson, The Physics of Solar Cells, Imperial College Press, Second Edition, 2003.
5. Manasreh, Semiconductor Heterojunctions and Nanostructures, McGraw Hill, First Edition 2005.

Code	Course	L	T	P	C
EC532	Low Power VLSI Design	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Compare various sources of power dissipation.

CLO2. Understand voltage scaling approaches for low power design.

CLO3. Apply adiabatic switching for low power design.

CLO4. Analyze switching activities involved in MOSFET's and different power dissipation mechanisms involved thereby.

CLO5. Design various low power designs such as Conditional Sum Adder, Carry Save adder etc.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	2	2	1	2
CLO2	3	2	3	2	-	1
CLO3	2	3	3	3	-	2
CLO4	3	2	3	3	1	3
CLO5	2	3	3	3	2	2

Syllabus Contents:

Module 1: Introduction: Introduction, Motivation for low power design, need and application low power design, Low power design space: voltage, Physical Capacitance, Switching Activity.

Module 2: Sources of power consumption and Power estimation: Static power and dynamic power: switching component of power, short circuit component of power, leakage component of power and other component of power consumption. Power estimation considering node transition activity factor, glitching effect and glitching power.

Module 3: Voltage Scaling approaches for low power design: reliability driven voltage scaling, technology driven voltage scaling, energy-delay minimum based voltage scaling, voltage scaling through threshold reduction, architecture driven voltage scaling. Concept of adiabatic charging, adiabatic amplification. Adiabatic logic gates, stepwise charging, pulsed power supply.

Module 4: Switching Capacitance minimization for low power design: Algorithmic approaches, Architecture optimization, Logic optimization, Circuit optimization, physical design optimization.

Module 5: Low power adder design: introduction, Standard adder: half adder, full adder, CMOS adder architectures: Ripple carry adder (RCA), Carry look- Ahead adder (CLA), Carry Select Adder (CSL), Carry Save Adder (CSA), Carry Skip Adder (CSK), Conditional Sum Adder (COS), Performances of all the adders with low power design, BiCMOS adders.

Textbooks:

1. Anantha P. Chandrakasan and Robert W. Broderick, “Low Power Digital CMOS Design”, Springer, First Edition 1995

Reference Books:

1. Kaushik Roy and Sarat C. Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley-IEEE Press, 2009
2. Kiat-Seng Yeo and Kaushik Roy, “Low – Voltage, Low – Power VLSI Subsystems”, McGraw-Hill Professional, 2004.

Code	Course	L	T	P	C
EC533	RF Design	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

- CLO1. Understand the basic and important concepts of RF Frequency.
- CLO2. Know about the passive components and design of transmission lines in RF frequency.
- CLO3. Understand the RF network theory related to semiconductor devices.
- CLO4. Analyze and design of RF Amplifier, oscillators.
- CLO5. Applications of filters, RF Amplifier.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	1	1	–	1
CLO2	3	2	2	2	1	2
CLO3	3	2	2	2	-	2
CLO4	2	3	3	3	2	3
CLO5	2	2	3	3	2	3

Syllabus Contents:

Module 1: Radio frequency concepts: Frequency spectrum and applications. Behaviour of passive components at radio frequencies, design parameters. RF Passive components: Passive RLC network, Distributed systems, Transmission lines and equivalent circuits. Design of transmission lines and transmission lines-based devices, Smith chart representation and Bandwidth estimation technique.

Module 2: RF Network theory: Interconnection of networks – Scattering parameters and properties – RF measurements and principles. Active RF components and modeling: Diode – Transistor – measurements of parameters – scattering parameter characterization.

Module 3: RF System Design: Impedance matching concepts – Microstrip matching – Transistor biasing networks – Amplifier design concepts and power relations – Design of portable systems.

Module 4: RF amplifier design: Voltage reference & biasing, Noise, LNA design, Mixers, RF power amplifiers, Feedback systems, Phase-locked loop, Oscillator, synthesizer, Phase noise, Resonant Circuits, Filter Design, Impedance Matching, The Transistor at Radio Frequencies, Small-Signal RF Amplifier Design, RF Power Amplifiers.

Text Books:

1. C.Y. Chang & S.M. Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.

2. S. K. Gandhi, VLSI Fabrication Principles, John Inc., New York, 1983.
3. S. M. Sze (Ed), VLSI Technology, 2nd edition, McGraw Hill, 1988.

Code	Course	L	T	P	C
EC534	RF Solid State Device	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

- CLO1. Understanding the basics of Semiconductor physics
- CLO2. Understanding the concept of transport mechanism in semiconductors
- CLO3. Understanding working concepts of RF active components.
- CLO4. Designing various Microwave Solid State Devices.
- CLO5. Analysis of various microwave devices.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO 1	3	2	2	2	1	2
CLO 2	3	2	3	2	-	1
CLO 3	2	3	3	3	-	2
CLO 4	3	2	3	3	1	3
CLO 5	2	3	3	3	2	2

Syllabus Contents:

Module 1: Energy Bands & Current Carriers in Semiconductors, Intrinsic & Extrinsic Semiconductor.

Module 2: Junction theory of Semiconductor, Carrier Process, Drift-Diffusion, Generation-Recombination.

Module 3: Microwave Transistor, Tunnel Diode, Microwave Field Effect Transistor.

Module 4: Transferred Electron Devices, Avalanche Transit Time Devices

Module 5: Optoelectronics, LED, Laser, Photo-detector, Solar Cell.

Textbooks:

1. Kanaan Kano, "Semiconductor Devices", Pearson, Fourth, 2021
2. B G Streetman & S Banerjee, "Solid State Electronic Devices, Pearson, Seventh, 2016
3. D A Neamen, Semiconductor Physics & Devices, Tata McGraw Hill, Fourth Edition, 2012

Reference Books:

1. S Y Liao, Microwave Devices & Circuits, Pearson, Third Edition 2003
2. Watson, Microwave Semiconductor Devices and their applications, McGraw Hill, First Edition, 1969
3. H.V. Shurmer, Microwave Semiconductors, Wien Oldenbourg, First Edition, 1965.

Code	Course	L	T	P	C
EC540	English for Technical Writing	2	0	0	2

Course Outcomes:

At the end of this course, students will be able to

CLO1. Develop vocabulary skills using word formation, prefixes, suffixes, synonyms, antonyms, and abbreviations.

CLO2. Apply effective writing techniques for clear, coherent, and grammatically correct communication.

CLO3. Identify and correct common grammatical and writing errors in technical documents.

CLO4. Demonstrate structured writing skills using description, definition, classification, and examples.

CLO5. Improve professional communication skills through reading, writing, listening, speaking, and presentations.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	2	1	2	1	-	-
CLO2	2	2	2	2	3	2
CLO3	1	-	-	2	2	2
CLO4	1	1	2	2	2	2
CLO5	2	3	2	2	3	3

Syllabus Contents:

Module 1: Vocabulary Building

The concept of Word Formation, Root words from foreign languages and their use in English, Acquaintance with prefixes and suffixes from foreign languages in English to form derivatives, Synonyms, antonyms, and standard abbreviations.

Module 2: Basic Writing Skills

Sentence Structures, Use of phrases and clauses in sentences, Importance of proper punctuation, Creating coherence, Organizing principles of paragraphs in documents, Techniques for writing precisely.

Module 3: Identifying Common Errors in Writing

Subject-verb agreement, Noun-pronoun agreement, Misplaced modifiers, Articles, Prepositions, Redundancies, Clichés.

Module 4: Nature and Style of sensible Writing

Describing, Defining, Classifying, providing examples or evidence, Writing introduction and conclusion.

Module 5: Writing Practices

Comprehension, Précis Writing, Essay Writing.

Module 6: Oral Communication

Listening Comprehension, Pronunciation, Intonation, Stress and Rhythm, Common Everyday Situations: Conversations and Dialogues, Communication at Workplace, Interviews, Formal Presentation.

References:

1. Effective Communication Skills, Kulbhushan Kumar, Khanna Book Publishing. 2022
2. Communication Skills in English, Anjana Tiwari, Khanna Book Publishing, 2022.
3. Practical English Usage. Michael Swan. OUP. 1995.
4. Remedial English Grammar. F.T. Wood. Macmillan.2007
5. On Writing Well. William Zinsser. Harper Resource Book. 2001
6. Study Writing. Liz Hamp-Lyons and Ben Heasley. Cambridge University Press. 2006.
7. Communication Skills. Sanjay Kumar and Pushpalata. Oxford University Press. 2011.
8. Exercises in Spoken English. Parts. I-III. CIEFL, Hyderabad. Oxford University Press.

Code	Course	L	T	P	C
EC541	Fundamentals of IoT	2	0	0	2

Course Outcomes:

At the end of this course, students will be able to

CLO1. Illustrate the fundamentals of IoT such as paradigms, architectures, possibilities, and challenges.

CLO2. Identify suitable hardware and interfaces for IoT deployments.

CLO3. Compare IoT protocols for communication.

CLO4. Develop cloud computing model and service options.

CLO5. Illustrate data analytics and security for IoT.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	-	2	1	-	-
CLO2	1	3	2	2	1	1
CLO3	1	2	3	2	1	2
CLO4	1	1	2	3	1	1
CLO5	1	1	2	2	3	3

Syllabus Contents:

Module 1: IoT Introduction and Fundamentals

Deciphering the term IoT Applications where IoT can be deployed Benefits/Challenges of deploying an IoT, IoT components: Digital Signal Processing, Data transmission, Choice of channel (wired/wireless), back-end data analysis. Understanding packaging and power constraints for IoT implementation.

Module 2: Signals, Sensors, Actuators, Interfaces

Introduction to sensors & transducers, Introduction to electrodes & biosensors, Static and dynamic characteristics of sensors, Different types of sensors, Selection criteria's for sensors / transducers, Commercial IoT sensors / transducers, Signal conditioning modules of IoT system, Energy and power considerations, Introduction to actuators, Different types of actuators, Interfacing challenges, Specification sheets of sensors / transducers, Specifications of actuators, Modules of data acquisition system, Wireless sensor node structure, positioning topologies for IoT infrastructure.

Module 3: Communication and Networking in IoT

Review of Communication Networks, Challenges in Networking of IoT Nodes, range, bandwidth Machine-to-Machine (M2M) and IoT Technology Fundamentals, Medium Access Control (MAC) Protocols for M2M Communications Standards for the IoT Basics of 5G

Cellular Networks and 5G IoT Communications, Low-Power Wide Area networks (LPWAN) Wireless communication for IoT: channel models, power budgets, data rates. Networking and communication aspects: IPv6, 6LoWPAN, COAP, MQTT, Operating Systems need and requirements for IoT.

Module 4: Modern networking

Cloud computing: Introduction to the Cloud Computing, History of cloud computing, Cloud service options, Cloud Deployment models, Business concerns in the cloud, Hypervisors, Comparison of Cloud providers, Cloud and Fog Ecosystem for IoT Review of architecture.

Module 5: IoT Data analytics and Security

OLAP and OLTP, NoSQL databases, Row and column Oriented databases, Introduction to Columnar DBMS CStore, Run: Length and Bit vector Encoding, IoT Data Analytics. Cryptographic algorithms, Analysis of Light weight Cryptographic solutions IoT security, Key exchange using Elliptical Curve Cryptography, Comparative analysis of Cryptographic Library for IoT.

Textbooks:

1. Arshdeep Bahga and Vijay Madisetti, “Internet of Things, a hands-on approach”, Universities Press (India) Pvt. Ltd. 2017, ISBN: 978-81-7371-954-7.
2. Rajkumar Buyya, Amir Vahid Dastjerdi, “Internet of Things Principles and Paradigms”, Copyright © 2016 Elsevier Inc., ISBN: 978-0-12-805395-9.

References:

1. William Stallings, “Foundations of Modern Networking: SDN, NFV, QoE, IoT, and Cloud” Publisher: Addison-Wesley 2015 ISBN: 9780134175393
2. Gaston C. Hillar, “Internet of Things with Python”.

**SEMESTER II
M.TECH.
IN
MICROELECTRONICS AND VLSI DESIGN**

Code	Course	L	T	P	C
EC506	VLSI Technology	3	0	0	3

Course Learning Outcomes:

At the end of this course, the students will be able to:

CLO1. Understand about clean room and its safety measures

CLO2. Learn about diffusion modeling and technology.

CLO3. Gain knowledge about oxidation process.

CLO4. Understand the process of chemical vapour deposition

CLO5. Explain the main challenges in fabrication industry and select suitable growth technique in a given range of constraints.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	1	-	-	1
CLO2	3	2	2	2	1	2
CLO3	3	2	2	2	1	2
CLO4	3	2	2	2	1	2
CLO5	3	3	3	3	2	3

Syllabus Contents:

Module 1: Environment for VLSI Technology: Clean room and safety requirements, Water cleaning processes & wet chemical etching techniques. Impurity incorporation: Solid state diffusion modeling & technology: Ion implantation modeling, technology & damage annealing, Characterization of impurity profiles.

Module 2: Oxidation: Kinetics of Silicon dioxide growth both for thick, thin & ultrathin films. Oxidation technologies in VLSI & ULSI: Characterization of oxide films; High K and low k dielectrics for ULSI. Lithography: Photolithography-beam lithography & newer lithography techniques for VLSI/ULSI; Mask Generation

Module 3: Chemical Vapor Deposition Techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride & metal films; Epitaxial growth of silicon; modeling & technology. Metal Film Deposition: Evaporation & sputtering techniques. Failure mechanisms in metal interconnects; multilevel metallization schemes.

Module 4: Plasma & Rapid Thermal Processing: PECVD, Plasma etching & RIE techniques; RTP techniques for annealing, growth & deposition of various films for use in ULSI.

Module 5: Process Integration for NMOS, CMOS & Bipolar Circuits: Advanced MOS technologies

Textbooks:

4. S. M. Sze, VLSI Technology, 2nd edition, McGraw Hill, 1988.

Reference Books:

1. C.Y. Chang & S.M. Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
2. S. K. Gandhi, VLSI Fabrication Principles, John Inc., New York, 1983.

Code	Course	L	T	P	C
EC507	Analog VLSI Design	3	0	0	3

Course Learning Outcomes:

At the end of this course, students will be able to:

CLO1. Understand thorough knowledge about CMOS, MOS devices.

CLO2. Analyse the single stage amplifier.

CLO3. Design 2-stage and folded cascade Op-Amp to meet the given specifications.

CLO4. Understand the theory and working principle of sample and hold circuit.

CLO5. Analyze the circuit of data converters

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	1	-	-
CLO2	3	2	3	3	2	3
CLO3	2	3	3	3	2	2
CLO4	3	2	2	2	1	1
CLO5	3	2	3	3	2	3

Syllabus Contents:

Module 1: Introduction to CMOS analog circuits, MOS transistor DC & AC small signal parameters from large signal model.

Module 2: Common source amplifier with various loads, source follower, common gate amplifier, cascade amplifier, folded cascade, frequency response, stability, and noise issues of amplifiers.

Module 3: Current/ source/ sink mirror. Matching, Wilson current source and regulated current source, Band-gap reference,

Module 4: Differential amplifier, Op-Amp, Design of Op-Amp, Sense amplifier

Module 5: Data Converters: Sample and Hold, Sampled Data Circuits, Switched capacitor filters, DAC, ADC.

Textbooks:

1. B Razavi, Design of Analog Integrated Circuits, Tata McGraw Hill, Second Edition, 2017
2. R. Jacob Baker, H.W. Li, and D.E Boyce CMOS Circuit Design, Layout and Simulation, Prentice- Hall of India, 1998

Reference Books:

1. B. Razavi, RF Microelectronics, Prentice Hall.
2. Mohammed Ismail and Terri Faiz, Analog VLSI Signal and Information Process, McGraw-Hill Book Company, 1994
3. Paul R. Gray and R.G Meyer, Analysis and design of Analog Integrated Circuits, John-Wily and sons, USA, (3rd Edition),1993
4. Journals: IEEE Journal of Solid State Circuits.

Code	Course	L	T	P	C
EC508	VLSI System Design and Verification	3	0	0	3

Course Learning Outcomes:

At the end of this course, students will be able to

CLO1. Familiarity of Front-end design and verification techniques and create reusable test environments.

CLO2. Design and verify combination and sequential circuits using HDL

CLO3. Design and verify complex designs based on given specifications

CLO4. Understand the verification guidelines for digital designs

CLO5. Analyze digital design using EDA tools like Cadence and Synopsys.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	2	3	3	3	2	2
CLO2	2	3	3	3	2	3
CLO3	1	3	3	3	2	2
CLO4	3	2	1	1	-	-
CLO5	3	2	3	3	2	3

Syllabus Contents:

Module 1: Design Concepts – Digital Hardware, Design Process, and Design of digital hardware, Introduction to CAD tools, and introduction to System Verilog. Logic system, data types and operators for modeling in System Verilog HDL. System Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection. Behavioral descriptions in SystemVerilog HDL.

Module 2: Synthesis of combinational logic – multiplexers, decoders, encoders, code converters, arithmetic comparison circuits, verilog/vhdl for combinational circuits. Synthesis of Sequential logic- Flip-Flops- SR, D, Master slave edge triggered D, T, JK, registers – shift registers, parallel access shift registers, counters – asynchronous, synchronous, counters with parallel load, reset synchronization, other counters, simple processor.

Module 3: Synchronous sequential circuits – basic design steps, state assignment problem, serial adder, state minimization, design of counter using the sequential circuit approach, FSM as an arbiter circuit, ASM.

Module 4: Verification guidelines - Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench. components, layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

Module 5: SystemVerilog Assertions, Basic OOP Introduction, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding

dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench, connecting testbench and design.

Textbooks:

1. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, PHI, 1999.
2. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

References:

1. Chris Spears, “System Verilog for Verification”, Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
3. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design, Specification, and Verification Language).
4. System Verilog website – www.systemverilog.org
5. OVM, UVM (on top of SV) www.verificationacademy.com

Code	Course	L	T	P	C
EC509	Analog VLSI Design Lab	0	0	2	1

Course Learning Outcomes:

At the end of this course, students will be able to

CLO1. Find the performance analysis of various analog circuits

CLO2. Simulate OP-amp, Comparator and their applications in schematic and layout level.

CLO3. Analyze various devices performance parameters in device simulator

CLO4. Innovate new device and verify the same in various circuits.

CLO5. Interpret simulation and experimental results to optimize analog VLSI circuit performance for practical applications.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	2	3	1	3
CLO2	3	3	3	2	-	2
CLO3	3	3	2	3	-	3
CLO4	2	3	3	3	2	3
CLO5	2	3	3	3	3	3

Syllabus Contents:

The laboratory course experiments are related to simulation of analog circuits using EDA Tool, and device simulation using TCAD tool.

1. Design of single stage amplifier
2. Design of current mirror
3. Design of differential amplifier
4. Design an Op-amp
5. Design of Comparator

Note: For the above experiments (1-5) complete the design flow as mentioned below:

- a) Draw the schematic and verify the following:
 - i) DC Analysis ii) AC Analysis iii) Transient Analysis
 - b) Draw the Layout and verify the DRC, ERC.
 - c) Check for LVS and Extract RC and back annotate the same and verify the design.
6. To design a Bulk MOSFET using TCAD and check its I_{ON}/I_{OFF} , SS and I_D vs. V_{GS} characteristics.
 7. To design a Double Gate MOSFET using TCAD and check its I_{ON}/I_{OFF} , SS and I_D vs. V_{GS} characteristics.
 8. To design a SOI MOSFET using TCAD and check its I_{ON}/I_{OFF} , SS and I_D vs. V_{GS} characteristics.
 9. To design a TFET using TCAD and check its I_{ON}/I_{OFF} , SS and I_D vs. V_{GS}

characteristics.

10. To design a HEMT using TCAD and check its I_{ON}/I_{OFF} , SS and I_D vs. V_{GS} characteristics.

Code	Course	L	T	P	C
EC510	VLSI System Design and Verification Lab	0	0	2	1

Course Learning Outcomes:

At the end of this course, students will be able to

- CLO1. Use Hardware Description Language SystemVerilog to design digital VLSI systems
- CLO2. Create testbench to verify the designs using various verification techniques
- CLO3. Design digital VLSI systems using FPGA design flow
- CLO4. Design digital VLSI systems using ASIC design flow
- CLO5. Analyze timing behavior, logic correctness, and performance parameters of VLSI circuits.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	3	2	1	-
CLO2	2	3	3	3	2	2
CLO3	2	3	3	3	-	2
CLO4	3	3	3	3	1	2
CLO5	3	2	2	3	2	3

Syllabus Contents:

1. Language semantics - Time Control: delay operator, event control. - Assignment Types: procedural, blocking, non-blocking, continuous. - Delay through combinational logic and nets
2. Implement half Adder/full adder using SystemVerilog.
3. Implement D/T Flip flop using SystemVerilog.
4. Design and Verification of ALU using SystemVerilog.
5. Design and Verification of Vending Machine using SystemVerilog.
6. Design and Verification of MIPS processor using SystemVerilog.
7. Entering design constraints, synthesis and implementation of designs using FPGA - Generating timing reports; CLB/gate usage reports.
8. Design and synthesis using ASIC EDA Tools - Generating timing, area, power reports
9. Static Timing Analysis of digital systems.
10. Floorplanning, Place & Route of digital systems.

Code	Course	L	T	P	C
EC550	AC Analysis of MOS	3	0	0	3

Course Learning Outcomes:

At the end of this course, students will be able to:

CLO1. Articulate the need for quasi-static operations of MOS.

CLO2. Interpret the fundamental behavior of MOS when excited by ac signal superimposed with DC bias supplies.

CLO3. Demonstrate frequency limitations of AC parameters of MOS.

CLO4. Identify various conductive and capacitive effects in various (low, medium, and high) frequency ranges.

CLO5. Express proficiency in general considerations and choices for common circuit simulation tools.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	1	-	-
CLO2	3	2	3	2	1	2
CLO3	3	2	3	2	1	2
CLO4	3	2	3	3	1	3
CLO5	2	3	3	3	2	2

Syllabus Contents:

Module 1: Large Signal modeling: Quasi-static operation, terminal currents in quasi-static operation, charge partitioning, charging currents, evaluation of intrinsic charges, transit time, limitations of quasi-static models, extrinsic capacitances and resistances, drain-source charge partitioning.

Module 2: Small Signal low frequency modeling: Intrinsic modeling: drain-to-source current, gate and body currents, complete low-frequency small signal model, various conductances in various regions of operations, effect of extrinsic resistances.

Module 3: Small Signal medium frequency modeling: Medium frequency small signal modeling for the intrinsic part, intrinsic transition frequency, small dimensional effects, noise analysis.

Module 4: High frequency small signal modeling: Quasi-static modeling: intrinsic capacitances, small signal equivalent circuit, capacitance evaluations. Non-quasi-static modeling and high frequency noise, RF modeling.

Module 5: Circuit simulation modeling: Various types of models, device modeling for circuit simulation, general considerations and choices, parameter extraction, introduction to common circuit simulation models.

Textbook(s):

1. Tsividis, Operation and modeling of the MOS transistor, McAndrew, Third Edition, 2013

Reference Books:

1. N. Arora, MOSFET Models for VLSI Circuit Simulation , Springer,1993.
2. Taur and Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, Third Edition, 2021.

Code	Course	L	T	P	C
EC551	Mixed Signal VLSI Design	3	0	0	3

Course Learning Outcomes:

At the end of this course, students will be able to:

CLO1. Design concepts and performance measures of mixed-mode VLSI design.

CLO2. Gain the concept of circuit design like the filters and comparators.

CLO3. Design the concepts of Sample and hold and trans-linear circuits.

CLO4. Design the principles related with data converters like the D/A converters and A/D converters.

CLO5. Analyze and design circuits like the Phase-locked loop.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	1	2	1	1
CLO2	3	2	1	1	-	-
CLO3	3	2	2	3	2	2
CLO4	3	3	3	3	3	2
CLO5	3	2	2	3	2	3

Syllabus Contents:

Module 1: Mixed-Signal design concepts and performance measures. Switched capacitor circuit- principles and applications in filter design- design of frequency and Q tunable continuous time filters. Comparators- Characterization - Two stage comparators - open loop comparators.

Module 2: Sample and hold and trans-linear circuits: Performance of sample-and-hold circuits - testing sample and holds, MOS sample-and-hold basics, examples of CMOS S/H Circuits, bipolar and BiCMOS sample-and-hold, trans-linear gain cell, trans-linear multiplier.

Module 3: Data converter fundamentals - DC and dynamic specifications - quantization noise - Nyquist rate D/A converters - decoder based converters - binary scaled converters - code converters - hybrid converters

Module 4: Advanced data converters: Nyquist rate A/D converters - Successive approximation, Flash, interpolating, Folding, Pipelined, Time-interleaved converters.

Module 5: Phase-locked loop basics; PLL dynamics; frequency synthesis; all-digital PLLs. Mismatch Issues in Analog Layouts, Introduction to RF IC Design.

Textbooks:

1. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley Inter-Science, 2003.
2. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, "Analog Integrated Circuit Design", Wiley, 2011.

References Books:

1. R.Gregorian and G.C.Temes, “Analog MOS Integrated Circuits for Signal Processing”, John Wiley and Sons, 2004.
2. Rudy van de Plassche, “CMOS integrated Analog- to Digital and Digital to- Analog converters”, Kluwer academic publishers, 2003.
3. P.E. Allen and D. R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2004.
4. Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill International Edition 2016.

Code	Course	L	T	P	C
EC552	Advanced Computer Architecture and Processor Design	3	0	0	3

Course Learning Outcome:

At the end of this course, students will be able to:

- CLO1. Have an idea of current challenges being faced in microprocessor design and the research trends to solve those problems.
- CLO2. Have a basic idea about ISA.
- CLO3. Comprehend memory design issues.
- CLO4. Acquire knowledge about multicore processor design issues.
- CLO5. Comprehend the concept of on chip networking.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	3	3	3	3
CLO2	3	1	1	1	-	-
CLO3	3	2	2	2	1	1
CLO4	3	1	2	2	1	1
CLO5	3	1	1	2	1	1

Syllabus Contents:

Module 1: Instruction Set Architecture (ISA) and Microarchitecture: ISA Principles and Trade-offs, RISC and CISC, Instruction Classes, Semantic Gap, Translation, MIPS and X86 ISA. Single Cycle and Multi Cycle Microarchitecture, Control and Data path.

Module 2: Pipelining: Pipelining basics, Ideal Pipeline, Pipeline Stalls, Data and Control Dependencies, Resource Contention, Data Dependence and Control Dependence handling.

Module 3: Branch Prediction: Misprediction penalty, BTB, Branch prediction techniques (Static and Dynamic), Out of Order Execution. SIMD Processing: Vector and Array Processors.

Module 4: The Memory Hierarchy: Memory System, DRAM and SRAM, Cache Memories, Direct mapped cache, Set-associative cache, Fully associative cache, Cache replacement policies, Cache Write Handling. Virtual Addressing: Basic Mechanism, Paging, Page Fault, Address translation, Page Replacement algorithms, Access Control, Privilege Levels.

Module 5: Multiprocessors: Parallel Speed-up, Amdahl's Law, Interconnects.

Textbook(s):

3. Hennessy and Patterson, Computer Architecture: A Quantitative Approach, Elsevier.

Reference Books:

1. Morris Mano, Computer System Architecture, Pearson.
2. Dally and Towels, Principal and Practices of Interconnection Networks, Elsevier

Code	Course	L	T	P	C
EC553	Solar Photovoltaics and Thin Film Technology	3	0	0	3

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1. Understand the concept of light and solar radiations

CLO2. Analyze the concept of solar cell.

CLO3. Understand the thin film technology solar cells and analyze its performance.

CLO4. Apply the fundamentals of solar cells for the development of emerging thin film solar cells.

CLO5. Design and analyze basic and emerging solar cells

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	1	1	1	-
CLO2	3	3	2	2	1	1
CLO3	3	2	2	3	2	3
CLO4	3	3	3	3	3	3
CLO5	3	2	3	2	3	2

Syllabus Contents:

Module 1: Basics of light and solar radiation: properties of light, energy of photon, photon flux, spectral irradiance, radiant powerdensity, black body radiation, sun radiation.Solar Radiation: declination angle, elevation angle, azimuth angle, the sun's position, solar radiation on a tilted surface, arbitrary orientation and tilt, calculation of solar insolation, measurement of solar radiation.

Module 2: Solar Cells: Evolution of solar cells, Basic principles of solar cell operation: electrical characteristics, optical properties, typical solar cell Structures, ideal efficiency.

Module 3: Crystalline Silicon Solar Cells: Manufacturing and properties of crystalline silicon, High efficiency laboratory cells, Screen-printed cells, Laser-processed cells, hit cell, rear-contacted Cells, thin silicon solarcells – light trapping, voltage enhancements, silicon deposition and Crystal growth.

Module 4: Thin-Film Solar Cells: Thin-film Silicon process technologies, hydrogenated amorphous silicon (a-Si:H)layers, Hydrogenated microcrystalline silicon (μ Si:H) layers, p-i-n and n-i-p structures, Tandem and Multi-junction solar cells.

Module 5: Emerging Thin-Film Solar Cells: CdTe based thin film solar cells, CuInSe₂ (CIS) based thin-film solarcells, CZTS Solar Cells-crystal structures, thin-film GaAs solar cells, Chalcopyrite based Solar Cells, Concentrator silicon solar cells, Dye-sensitized thin-film solar cells, Perovskite Solar Cell, Organic solarcells, Nanowire Solar Cells.

Textbooks:

1. Adrian Kitai, Principles of Solar Cells, LEDs and Diodes: The role of the PN junction, John Wiley & Sons, 2011.
2. Augustin McEvoy, L. Castaner, Tom Markvart, Solar Cells: Materials, Manufacture and Operation, 2nd edition, Newnes, 2012.

References

3. Arvind Shah, Thin-Film Silicon Solar Cells, Illustrated edition, EPFL Press, 2010.
4. I. M. Dharmadasa, Advances in Thin-Film Solar Cells, Illustrated edition, CRC Press, 2012.
5. P. Jayarama Reddy, Solar Power Generation: Technology, New Concepts & Policy, Illustrated edition, CRC Press, 2012.
6. A. Martí, A. Luque, Next Generation Photovoltaics: High Efficiency through Full Spectrum Utilization, Illustrated edition, CRC Press, 2010.
7. Ana Belén, Cristóbal López, Antonio Martí Vega, Antonio Luque López, Next Generation of Photovoltaics: New Concepts, Illustrated edition, Springer, 2012.
8. M. A. Green, Third Generation Photovoltaics: Advanced Solar Energy Conversion, Springer, 2006.

Code	Course	L	T	P	C
EC554	5G Communication Technology	3	0	0	3

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1. Understand and explain the channel models of 5G and the use cases for 5G.

CLO2. Analyze use of MIMO in 5G and its techniques.

CLO3. Draw and explain 5G architecture, its components and functional criteria.

CLO4. Understand device to device (D2D) communication and standardization.

CLO5. Understand 5G radio access technologies and interference management, mobility management and security issues in 5G.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	1	-	1	-
CLO2	3	3	1	2	2	2
CLO3	3	2	2	2	2	3
CLO4	3	1	1	1	1	1
CLO5	3	2	1	1	1	1

Syllabus Contents:

Module 1: Introduction to Wireless Communication: Fundamentals of Wireless Communication, Evolution of Wireless Communications and standards from 2G to 5G, Spectrum Analysis and Sharing for 5G.

Module 2: 5G Wireless Propagation Channels: Channel modeling requirements, Propagation scenarios and challenges in the 5G modeling, Relaying multi-hop and cooperative communications: Principles of relaying, fundamentals of relaying, Cognitive radio: Architecture, spectrum sensing, Software Defined Radio (SDR).

Module 3: MIMO systems: Introduction to Multi-antenna Systems, Motivation, Types of multi-antenna systems, MIMO vs. multi-antenna systems, Diversity, Exploiting multipath diversity, Transmit diversity, Space-time codes, The Alamouti scheme, Delay diversity, Cyclic delay diversity, Space-frequency codes, Receive diversity, The rake receiver, Combining techniques, Spatial Multiplexing.

Module 4: D2D: From 4G to 5G, D2D standardization: 4G LTE D2D, D2D in 5G: research challenges, Radio resource management for mobile broadband D2D, RRM techniques for mobile broadband D2D, RRM and system design for D2D, 5G D2D RRM concept: an example, Multi-hop D2D communications for proximity and emergency, services, National security and public safety requirements in 3GPP and METIS, Device discovery without and with network assistance.

Module 5: Transmission and Design Techniques for 5G: Basic requirements of

transmission over 5G, Modulation Techniques-Orthogonal frequency division multiplexing (OFDM), Generalized frequency division Multiplexing (GFDM), Filter Bank Multi-Carriers (FBMC), Universal filtered multi-carrier (UFCM). Multiple Accesses Techniques-Orthogonal Frequency Division Multiple Accesses (OFDMA), Generalized Frequency Division Multiple Accesses (GFDMA). Non-Orthogonal Multiple Accesses (NOMA).

Textbooks:

1. 5G Mobile and Wireless Communications Technology, Afif Osseiran, Jose F. Monserrat, Patrick Marsch, Cambridge University Press.
2. Fundamentals of 5G Mobile Networks, Jonathan Rodriguez, Wiley

References:

1. 5G NR: The Next Generation Wireless Access Technology, Erik Dahlman, Stefan Parkvall, Johan Sko'ld, Elsevier.

Code	Course	L	T	P	C
EC560	System on Chip Design	3	0	0	3

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1. Identify and formulate a given problem in the framework of SoC based design approaches.

CLO2. Design SoC based system for engineering applications.

CLO3. Realize impact of SoC on electronic design philosophy and macro-electronics thereby incline towards entrepreneurship & skill development.

CLO4. Understand low power techniques of SoC design

CLO5. Analyze performance of single core and multi core systems

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	3	3	2	2
CLO2	3	2	3	2	3	2
CLO3	3	1	3	2	2	2
CLO4	3	3	1	2	2	2
CLO5	3	2	1	1	1	1

Syllabus Contents:

Module 1: ASIC-Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Module 2: NISC-NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC) - design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Module 3: Simulation-Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Module 4: Low power SoC design / Digital system, - Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Module 5: Synthesis - Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for

synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.

Textbooks:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011.

References:

1. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.
2. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000.
3. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008.

Code	Course	L	T	P	C
EC561	Reconfigurable Hardware Design	3	0	0	3

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1: Comprehend the recent paradigm of Computing which offers flexibility, scalability and performance.

CLO2: Comprehend the concept of system/circuit redesign on the fly using dynamic reconfiguration.

CLO3: Optimize the given system specific to underlying reconfigurable hardware.

CLO4: Fetch the notion of evolvable circuit on Reconfigurable hardware.

CLO5: Develop and implement FPGA-based applications using hardware/software co-design and multi-FPGA reconfigurable systems for real-time applications.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	2	-	-
CLO2	3	2	2	3	1	2
CLO3	2	3	3	3	2	3
CLO4	2	2	3	2	1	2
CLO5	2	3	3	3	2	3

Syllabus Contents:

Module 1: Introduction to Reconfigurable Computing: Paradigms of computing.

Module 2: Reconfigurable Configurable Hardware: Device Architecture, Reconfigurable Computing Architecture, Reconfigurable Computing Systems, Reconfigurable Management.

Module 3: Programming Reconfigurable Systems: Compute Models and System Architectures, Programming

FPGA Applications in HDLs, Spatial Computing, Stream computations, Data parallel FPGA applications, Operating System Support for Reconfigurable Computing.

Module 4: Mapping Designs to Reconfigurable Platforms: Technology Mapping, FPGA Placement, Datpath Composition.

Module 5: Application Development: Implementing Applications with FPGAs, Hardware/software Partitioning, Multi-FPGA Systems: Logic Emulation Evolvable FPGAs, Network Packet Processing in Reconfigurable Hardware.

Texts/References:

1. Scott Hauck André DeHo, Reconfigurable Computing, 1st Edition, Morgan Kaufmann, eBook ISBN: 9780080556017, Hardcover ISBN: 9780123705228.
2. M. Gokhale and P. Graham, Reconfigurable Computing: Accelerating Computation with Field Programmable Gate Arrays, Springer, 1st Edition, 2005, ISBN: 978-0-387-

26105-8.

3. N. Voros and K. Masselos (eds.), System-Level Design of Reconfigurable Systems-on-Chip, Springer, 1st Edition, 2005, ISBN: 978-0387261034.
4. C. Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications, Springer, 1st Edition, 2007, ISBN: 978-1402060885.
5. P. Lysaght and W. Rosenstiel (eds.), New Algorithms, Architectures and Applications for Reconfigurable Computing, Springer, 1st Edition, 2005, ISBN: 978-1402031274.

Code	Course	L	T	P	C
EC562	Advanced CMOS Devices and Technology	3	0	0	3

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1: Understand the fundamentals of CMOS technologies and their structure, the scaling rules, and the power crisis.

CLO2: Analyze the High-K dielectric with respect to gate oxide.

CLO3: Understand the SOI device Technology considering fully depleted and partially depleted case.

CLO4: Have basic knowledge of multigate device physics.

CLO5: Apply the concept of benchmarking analog and digital models and lay outing.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	1	2	2	1	1
CLO2	3	2	2	3	1	2
CLO3	3	2	3	3	-	2
CLO4	2	2	3	2	-	2
CLO5	2	3	3	3	2	3

Syllabus Contents:

Module 1: Fundamentals: History of Si technology, Review of CMOS scaling. Problems with traditional geometric scaling. Power crisis. Review of basic quantum mechanics. Mobility enhancement techniques. Review of stress and strain, how it affects band structure of silicon. Types and realization of stress elements. Problems with stress elements.

Module 2: High-K Gate Dielectric and process: Gate oxide scaling trend. Urgency to switch gate dielectric material. High K material selection. Fermi level pinning Process integration of high K gate dielectrics and metal gates Multi-gate transistors. Ways of realization. Fabrication issues and integration challenges.

Module 3: SOI Devices: Basic principle of MOSFETs, Introduction to classical planer bulk MOSFETs, VMOS devices. Introduction to SOI Technology, radiation hardness capability. Partially depleted SOI MOSFET, Fullydepleted SOI MOSFET. Single gate SOI MOSFET, Double Gate SOI MOSFET, kink effect, Floating Body effect, Applications of SOI MOSFET, Comparison with Classical planer bulk MOSFET.

Module 4: Multigate CMOS devices: Introduction to Finfets, Ways of realization, Fabrication issues and integration challenges.

Module 5: CMOS compatible memory devices: Analog and digital benchmarking of models. Layout dependent effects. Test structures used for characterization, Variations and how it can affect scaling. Basics of sub wavelength lithography. Design for manufacturability.

References:

1. Hei Wong, “Nano-CMOS Gate Dielectric Engineering,” CRC, 2011.
2. J.P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer, 2010.
3. B. Wong, A. Mittal, Y. Cao, G. Starr, “Nano-CMOS Circuit and Physical Design”, Wiley Inter-science 2004.
4. A. Dimoulas, E. Gusev, P. McIntyre, M. Heyns, “Advanced Gate Stacks for High-Mobility Semiconductors”, Springer 2007.

Code	Course	L	T	P	C
EC563	Flexible Electronics	3	0	0	3

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1: Select appropriate materials and manufacturing methods to design a process flow for fabricating flexible electronic devices.

CLO2: Apply the fundamentals of electronic properties and role of interface in flexible and printed circuit systems.

CLO3: Explain the working principles of flexible devices like display, memory, photovoltaic cells and sensors

CLO4: Distinguish the electrical and mechanical properties of thin film transistors.

CLO5: Interpret the main challenges in materials and process selection, and circuit design for deformable circuitry.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	2	3	3	1	2
CLO2	3	1	3	3	-	2
CLO3	3	1	2	2	-	2
CLO4	3	2	3	2	1	3
CLO5	3	2	3	3	2	3

Syllabus Contents:

Module 1: Flexible Electronics Basics: Introduction to Flexible and Printed Electronics and their Materials Systems, Background and history, emerging technologies, general applications, Review of Semiconductors and Circuit Elements, Carrier transport, doping, band structure, thin-film electronic devices.

Module 2: Flexible Devices Fabrication and Materials: Thin-film Deposition and Processing Methods for Flexible Devices, CVD, ECVD, PVD, etching, photolithography, low-temperature process integration, Materials for Flexible and Printed Electronics: Nanowire and nanoparticle synthesis, transition metal oxides, amorphous thin films, polymeric semiconductors, paper-based electronics, textile substrates, barrier materials.

Module 3: Thin Film Transistors: Thin Film Transistors device structure and performance: I-V characteristics, Mechanics of Thin films and Flexible Thin film Transistors: thin film mechanics models, neutral plane, conformal electronics, mechanical modelling.

Module 4: Patterning Process, Interfaces: Solution-based Patterning Processes: Ink-jet printing, gravure, imprint lithography, spray pyrolysis, surface energy effects, multilayer patterning Contacts and Interfaces to Organic and Inorganic Electronic Devices: Schottky

contacts, defects, carrier recombination, effect of applied mechanical strain.

Module 5: Applications: Flexible Electronics Applications: Displays, sensor arrays, memory devices, MEMS, lab-on-a chip, and photovoltaics, Introduction to Cost Models and Economics of Printed Flexible Electronics: Overview of display industry cost models, cost advantages and disadvantages for printed electronics, scaling of large-area flexible systems, cost of goods sold for display applications.

Textbooks:

1. Wong, William S., Salleo, Alberto (Editors), Flexible Electronics: Materials and Application, Springer U.S./India – 2009 – ISBN: 9781441944948, DOI: 10.1007/978-0-387-74363-9.

References:

1. Guozhen Shen, Zhiyong Fan (Editor) - Flexible Electronics: From Materials to Devices, WorldScientific, U.S., 2016, ISBN: 9789814651981
2. Takao Someya (Editor), Stretchable Electronics, Wiley International, U.S., 2013, ISBN:9783527329786.

Code	Course	L	T	P	C
EC571	IKS in Electronics Engineering	2	0	0	2

Course Learning Outcomes:

At the end of the course, students will be able to:

CLO1: Explain the historical development and major contributions of Indian mathematics, including number systems, algebra, geometry, and astronomy.

CLO2: Describe the mathematical concepts developed by ancient and medieval Indian mathematicians and their influence on modern mathematics.

CLO3: Analyze the structure, features, and growth trends of the Indian economy in the context of agriculture, industry, and services sectors.

CLO4: Interpret key economic indicators such as GDP, inflation, unemployment, fiscal policy, and monetary policy related to the Indian economy.

CLO5: Evaluate the role of mathematical thinking and economic principles in addressing contemporary societal, technological, and developmental challenges in India.

CLOs and PLOs Mapping:

CLOs/PLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	3	-	1	1	-	2
CLO2	3	-	2	1	1	2
CLO3	2	-	1	3	1	3
CLO4	2	-	1	3	1	3
CLO5	3	-	2	3	2	3

Syllabus Contents:

Module 1: The Introduction to Ancient Mathematics

Introduction to Brief introduction of inception of Mathematics from vedic periods. Details of different authors who has given mathematical & astronomical sutra (e.g. arytabhatta, bhaskara, brahmagupta, varamahira, budhyana, yajanvlkya, panini, pingala, bhara muni, sripati, mahaviracharya, madhava, Nilakantha somyaji, jyeshthadeva, bhaskara-II, shridhara) Periodical enlisting of Mathematical & Astrological achievement in India. Evolution of Indian Numerals (Brahmi (1st century), Gupta (4th century) & Devanagri Script (11th century).

Module 2: Ancient Mathematics –I

Veda & Sulvasutras (Pythagoras theorem, Square root & Squaring Circle) (baudhayana sulbhasutra, apastamba sulbhasutra, katyayana sulbhasutra, manava sulbhasutra, maitrayana sulbhasutra, varaha sulbhasutra, vadhula sulbhasutra, Pingala's chandasutras, sunya, yaat-tavat, Aryabhata (Aryabhatiya, Asanna, ardha-jya, kuttaka,), bhaskara (trigonometry,shridhara, mahavira), Bhaskara Acharya (Sidhantashiromani), Varamahira panchasiddhantika.

Module 3: Ancient Mathematics –II

Brahmagupta (vargaprakrati, bhramasphuta siddhanta, bhavana), ayatavrtta, ganitasarasamgraha, lilavathi, ganesadaivajna, randavantika, suryasidhhanta, grahalaghava, sadratnamala, mandavrtta, sigrharrta, Bijaganita, Bakshali manuscript Golavada, Madhyamanayanaprakara, Mahajyanayanaprakara (Method of Computing Great Sines), Lagnaprakarana, Venvaroha, Sphutacandrapti, Aganita-grahacara, Chandravakyani (Table of Moon-mnemonics)

References:

1. Textbook on IKS by Prof. B Mahadevan, IIM Bengaluru.
2. R P Kulkarni, Glimpse of Indian Engineering and Technology (Ancient & Medieval period, Munshiram Manoharlal Publishers Pvt. Ltd. 2018.
3. AK Pathak, Science and Technology in India, Anshika prakashan pratapgarh, 2016
4. NVP, Unithiri, Indian Scientific Traditions (Professor K.N. Neelakantan Elayath 287 Model curriculum for UG Degree in BBA Felicitation Volume), publication division univeristy of Calicut, 2006
5. Dharmpal, Indian science and technology in the eighteen century, rashtrottahana sahitya, 1983
6. S Biswal, B L ray, vedic Science and technology, DK Print world, 2009
7. A Kolachana, Studies in Indian Mathematics and Astronomy, Hindustan Book agency
8. S B Rao, Indian Mathematics and Astronomy: Some Landmarks (Revised Third Edition), Bhartiya Vidhya Bhavan, 2012,
9. GG Josheph, Indian Mathematics: Engaging with the World from Ancient to Modern Times, speaking Tiger, 2016
10. BS Yadav, Ancient Indian Leaps into Mathematics, brikausher publication, 2010
11. DP Chatopadhyaya, Ravinder kumar, Mathematics, Astronomy, and Biology in Indian Tradition: Some Conceptual Preliminaries (Phispc Monograph Series on History of Philosophy, Science and Culture in India, No 3), Munshiram manoharlal publication, 1995
12. BV subbarayappa, The Tradition of Astronomy in India: History of Science, Philosophy and Culture in Indian Civilization Vol. IV, Part 4: Jyotihshastra (History of Science, Philosophy & Culture in Indian Civilization), centre for studies in civilization, 2008
13. GE Clark, The Aryabhata of Aryabhata: An Ancient Indian Work on Mathematics and Astronomy, Kesinger publicaiton, 2010
14. Anonyms, Hindu Astronomy: Anuradha, Bharani, Hindu Chronology, Hindu Calendar, Indian Astronomy, Kerala School of Astronomy and Mathematics, Jyoti, Book LLC, 2011
15. KV Sharma. Ganita yuktibhasa (Analytical Exposition of the Rationales of Indian Mathematics and Astronomy, Kindle, 2021.

Code	Course	L	T	P	C
EC572	Introduction to Drone Technology	2	0	0	2

Course Outcomes:

At the end of this course, students will be able to

CLO1. Learn about various types of drones.

CLO2. Identify and understand the various components of drone design.

CLO3. Design basic drone systems.

CLO4. Apply principles of flight mechanism and dynamics.

CLO5. Analyze diverse drone applications.

CLOs and PLOs Mapping:

CLO/PLO	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6
CLO1	2	-	-	-	-	3
CLO2	1	2	3	-	3	-
CLO3	3	3	2	2	-	-
CLO4	3	2	2	-	1	-
CLO5	1	-	-	-	-	3

Syllabus Contents:

Module 1: Introduction to Drones

Definition and history of drones, Types of drones and their applications, Drone components and terminology, Regulations and Guidelines for drone usage.

Module 2: Drone Design and Assembly

Design considerations for drone airframe and propulsion systems, Selecting and assembling drone components such as motors, batteries, flight controllers, and cameras, Basic wiring and soldering techniques.

Module 3: Drone Motors and ESC

Working, Types: Brush and Brushless Motors, motor sizing and identification, mounting patterns and thread size, Thrust to Weight ratio, KV ratings, advanced motor selection, Electronic Speed Controller (ESC)

Module 4: Flight Mechanics and Dynamics

Basic principles of flight mechanics, flight controller board, Selection of drone controller with example, Factors affecting drone flight performance and efficiency.

Module 5: Applications of Drone

Overview of commercial and industrial drone applications, Case studies and examples of successful drone deployments, GPS based navigation system, Drone Camera Systems, Agro application, Drone Delivery, Future trends and developments in the drone industry.

Text Books:

1. M. LaFay, Building Drones for Dummies, John Wiley & Sons, Inc., n.d.
2. E. Tooley, Practical Drones: Building, Programming, and Applications, Apress, 2021.
3. D. Levy, Drone Programming: A Guide to Code Your Own Drones, Packt Publishing, n.d.
4. S. K. Koppa, Drone Technology: Theory and Practice, Springer, 2020.
5. P. Horowitz and W. Hill, The Art of Electronics, Cambridge University Press, 2015.
6. K. Sundar and R. V. Rajakumar, Multicopters: Principles and Applications, Springer, 2021.

References:

1. D. Saxby, Drone Aerial Photography and Video: Techniques and Stories from the Field, Cengage Learning, 2018.
2. D. McLeod, Getting Started with Drone: How to Build, Fly, and Program Your Own Drone, Apress, 2019.
3. M. A. Banks, Building and Flying Electric Model Aircraft, O'Reilly Media, Inc., 2014.
4. G. C. Camara Leal, Flying Robots: An Introduction to Autonomous Aerospace Systems, Springer, 2017.